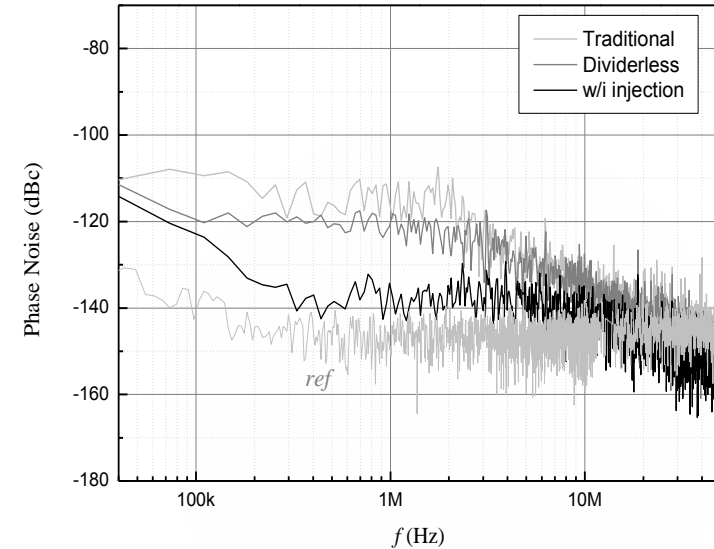
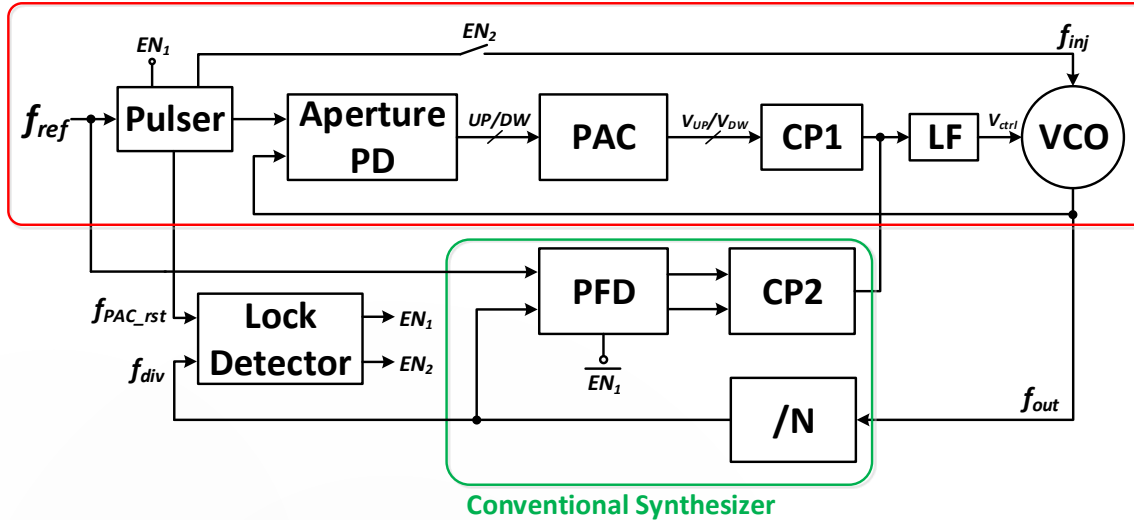


# A Dividerless Subharmonically Injection Locked PLL with Self Injected Signal Aligning

## Main Loop



## ◆ Conventional Synthesizer

- Provides frequency locking in the first condition.

## ◆ Lock Detector

- Switches the circuit to dividerless loop while frequency locked, or to conventional synthesizer while unlocked.
- Turns on the injection path after the Dividerless loop operates a long duration.

## ◆ Dividerless PLL

- Directly compares the phase difference between VCO signal and injection signal, which provides a more ideal injection condition than usual.

## ◆ Subharmonically Injection Locked PLL

- Reduces the inband phase noise, by injecting clear signal into VCO under phase aligned condition provided by dividerless PLL.

Simulation results	Dividerless	Injection locked
Freq. (GHz)	2.4	
Tech. (nm)	180	
Pref. (MHz)	100	
Ref Spur (dBc)	-50	-38
PN. @100kHz(dBc)	-120	-122
PN. @1MHz(dBc)	-122	-135
RMS Jitter (fs)	136 (50kHz-80MHz)	43.8 (50kHz-80MHz)
SupplyVoltage (V)	1.8	
Power (mW)	28.8	57.2